REMARKS

This communication is a full and timely response to the aforementioned non-final Office Action dated February 11, 2009. By this communication, claims 1, 2, 14-17, 19, 21 and 22 are amended, and claim 23 is cancelled. Claims 3-13, 18 and 20 are not amended and remain in the application. Thus, claims 1-22 are pending in the application. Claims 1 and 14-17 are independent.

Reconsideration of the application and withdrawal of the rejections of the claims are respectfully requested in view of the foregoing amendments and the following remarks.

I. Rejections Under 35 U.S.C. § 103(a)

A. Claims 1, 4, 12-18 and 21-23 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Inaba et al. (U.S. Patent No. 5,477,557, hereinafter "Inaba") in view of Nagarajan et al. (U.S. Patent No. 5,760,939, hereinafter "Nagarajan").

Without acquiescing to this rejection, independent claims 1 and 14-17 have each been amended to emphasize distinctions between the claimed invention and the applied references. Applicants respectfully submit that the claimed invention is patentable over the applied references for at least the following reasons.

As illustrated in Figure 1, for example, an exemplary embodiment of the present invention provides an optical semiconductor device that comprises an optical semiconductor element (e.g., laser diode (LD) 20) having a cathode and an anode. The optical semiconductor device also comprises a first conductor line connected to the cathode of the optical semiconductor element, and supplying a first electric signal (e.g., positive phase signal) to the optical semiconductor element (e.g., LD 20). The optical semiconductor device also comprises a second conductor line connected to the anode of the optical semiconductor element (e.g., LD 20), and supplying a second electric signal (e.g., anti-phase signal) to the optical semiconductor element (e.g., LD 20).

The optical semiconductor device of the exemplary embodiment also comprises a first inductance element (e.g., solenoid 21a) connected to the cathode of the optical semiconductor element (e.g., LD 20) and the first conductor line. In

addition, the exemplary optical semiconductor device comprises a second inductance element (e.g., solenoid 21b) connected between the anode of the optical semiconductor element (e.g., LD 20) and a ground potential (e.g., the ground potential above the upper horizontal dotted line denoting LD module 2) such that one end of the second inductance element (e.g., solenoid 21b) is connected at the ground potential. The disclosed embodiment provides that the second inductance element (e.g., solenoid 21b) is also connected to the second conductor line.

The disclosed embodiment also provides that the first and second conductor lines constitute a pair of differential lines. In addition, with reference to line 2 on page 20 to line 18 on page 21 of the specification, the exemplary embodiment provides that the first and second inductance elements (e.g., solenoids 21a, 21b) are configured to permit a bias current (e.g., from the ground potential to negative power supply Vee through LD module 2) to pass therethrough, and simultaneously prevent the first and second electric signals from passing therethrough, respectively.

As described in the paragraph beginning at line 2 on page 20, the solenoids 21a and 21b can be constituted, for example, by air-cored coils which cause bias currents (direct currents (DC)) to pass through, and which suppress modulated signals (electric signals) output from the LD driving circuit 1 from leaking from the first and second bias circuits 28a and 28b. In other words, the solenoids 21a and 21b respectively cut off the first and second electric signals and thereby prevent the first and second electric signals (modulated signals) from leaking, because the solenoids 21a and 21b respectively prevent the first and second electric signals from passing therethrough.

In addition, with reference to Figure 1, for example, the exemplary embodiment provides that the second inductance element (e.g., solenoid 21b) is connected between the anode of the optical semiconductor element (e.g., LD 20) and a ground potential such that one end of the second inductance element (e.g., solenoid 21b) is connected at the ground potential. For instance, as shown in Figure 1, for example, one end of the second inductance element (e.g., solenoid 21b) is connected to a ground potential and is therefore connected at the ground potential.

Accordingly, the above-described exemplary embodiment provides that inductance elements are connected to both the cathode and the anode of the optical

semiconductor element (e.g., LD 20), and that both the first and second conductance elements are configured to permit a bias current to pass therethrough, and simultaneously prevent the first and second electric signals from passing therethrough, respectively.

Independent claims 1 and 14-17 recite various features of the above-described exemplary embodiment.

In particular, claims 1 and 14, 15 and 17 each recite that the optical semiconductor element has a cathode and an anode, and that the second inductance element is connected between the anode of the optical semiconductor element and a ground potential such that one end of the second inductance element is connected at the ground potential. Furthermore, claims 1 and 14, 15 and 17 each recite that the first and second inductance elements are configured to permit a bias current to pass therethrough, and simultaneously prevent the first and second electric signals from passing therethrough.

Claim 16 recites that the optical semiconductor element has a cathode and an anode, and that the second bias circuit is electrically connected to the second terminal, between the anode of the optical semiconductor element and a ground potential such that one end of the second bias circuit is connected at the ground potential. In addition, claim 16 recites that the first and second bias circuits are configured to permit a bias current to pass therethrough, and simultaneously prevent the first and second differential signals from passing therethrough, respectively.

Applicants respectfully submit that the applied references do not disclose or suggest all the recited features of the claimed invention for at least the following reasons.

With reference to Figure 2, Inaba discloses a pair of transistors Q1 and Q2 whose collectors are connected by a semiconductor laser LD. The anode of the semiconductor laser LD is connected to the collector of transistor Q1, and the cathode of the semiconductor laser LD is connected to the collector of transistor Q2. An inductor is connected between the cathode of the semiconductor laser LD and the transistor Q1 (see Column 2, lines 14-25, and Column 3, lines 15-25).

In an attempt to arrive at the claimed invention, the Office alleged that:

(1) the semiconductor laser LD of Inaba corresponds to the optical semiconductor element of claim 1,

(2) the wiring between the cathode of the semiconductor laser LD and the collector of transistor Q1 corresponds to the first conductor line of claim 1,

(3) the wiring between the collector of transistor Q2 and the anode of the semiconductor laser LD of Inaba corresponds to the second conductor line of claim 1, and

(4) the sole inductor of Inaba corresponds to the first inductance element of claim 1.

However, as acknowledged by the Office, Inaba does not disclose or suggest the second inductance element as recited in claim 1. Specifically, as acknowledged by the Office, Inaba does not disclose or suggest an inductance element connected between the anode of the semiconductor laser LD and the ground potential connected to the wiring between the collector of transistor Q2 and the anode of the semiconductor laser LD.

With the claimed invention as a road map, the Office applied Nagarajan in an attempt to cure the deficiencies of Inaba for failing to disclose or suggest the second inductance element as recited in claim 1.

As illustrated in Figure 2, Nagarajan discloses a driver 12 for driving a laser diode LD 14. A cathode of the LD 14 is connected to a resistor and an inductor in parallel. The Office referred to the combination of the resistor and inductor connected to the cathode of LD 14 as a "low pass RL filter." The Office alleged that it would have been obvious to one of ordinary skill in the art "to combine the circuit of Inaba with the low pass RL filter of Nagarajan in order to provide for an RF block to keep interference from occurring with the DC driving."

Applicants respectfully submit that this assertion is not supportable and is contrary to the disclosure of the applied references. In particular, neither Inaba nor Nagarajan disclose, suggest or contemplate providing an inductance element between the cathode of a laser diode and a conducting line, in combination with an inductance element between the anode of a laser diode and a ground potential.

On the contrary, Inaba and Nagarajan merely disclose an inductor between the cathode of the laser diode and a conducting line.

In the second paragraph on page 5 of the Office Action, the Office asserted that "the first/second electrode labeling of the respective anode and cathode does not affect the connections limited by the claim language." This assertion is not supportable for numerous reasons. First, the terms "anode" and "cathode" are not merely "labels" as suggested by the Office. Rather, the terms "anode" and "cathode" have well-defined meanings in the art. For instance, the term "anode" means an electrode through which an electric charge flows in an optical semiconductor element (e.g., a laser diode). Conversely, the term "cathode" means an electrode through which an electric charge flows out of an optical semiconductor element (e.g., a laser diode). Accordingly, the terms "anode" and "cathode" are more than just "labels" that the Office appears to want to disregard in order to reject the claimed invention.

Second, the disclosure of the applied references does not support the Office's assertion that the "labeling" of the cathode and anodes in claim 1 "does not affect the connections limited by the claim language." The applied references refute this assertion. In particular, both Inaba and Nagarajan fail to disclose or suggest an inductance element connected between the anode of their respective laser diode and a ground potential.

Furthermore, modifying Inaba to provide an inductance element between the ground potential and the anode of the semiconductor laser LD would serve to diminish the bias voltage of the semiconductor laser LD, and thereby diminish the efficacy of the semiconductor laser LD.

Accordingly, Applicants respectfully submit that Inaba and Nagarajan each fail to disclose or suggest the second inductance element is connected between the anode of the optical semiconductor element and a ground potential such that one end of the second inductance element is connected at the ground potential, where the first and second inductance elements are configured to permit a bias current to pass therethrough, and simultaneously prevent the first and second electric signals from passing therethrough, as recited in claims 1, 14, 15 and 17.

Similarly, Applicants respectfully submit that Inaba and Nagarajan each fail to disclose or suggest the second bias circuit being electrically connected to the second

terminal, between the anode of the optical semiconductor element and a ground potential such that one end of the second bias circuit is connected at the ground potential, where the first and second bias circuits are configured to permit a bias current to pass therethrough, and simultaneously prevent the first and second differential signals from passing therethrough, respectively, as recited in claim 16.

Moreover, for the reasons presented above, Applicants respectfully submit that, contrary to the Office's unsupported assertion, it would not have been obvious to one skilled in the art to modify the circuit of Inaba with the inductor connected to the cathode of the laser diode LD of Nagarajan.

Accordingly, for at least the foregoing reasons, Applicants respectfully submit that claims 1 and 14-17 are patentable over Inaba and Nagarajan, since Inaba and Nagarajan, either individually or in combination, fail to disclose or suggest all the recited features of claims 1 and 14-17.

B. Dependent claims 2, 3, 5 and 19-20 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Inaba and Nagarajan in view of Nagahori, Takeshi et al. ("An Analog Front-End Chip Set Employing an Electro-Optical Mixed Design on SPICE for 5-Gb/s/ch Parallel Optical Interconnection." IEEE Journal of Solid-State Circuits, Volume 36, No. 12, pp 1984-1994, December 2001, hereinafter "Takeshi"). Dependent claim 6 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Inaba, Nagarajan, Takeshi and further in view of Ito et al. (U.S. Patent No. 4,975,664, hereinafter "Ito").

In addition, dependent claims 7-9 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Inaba, Nagarajan, Takeshi, Ito and further in view of Kobayashi et al. (U.S. Patent No. 5,982,793, hereinafter "Kobayashi"). Lastly, dependent claims 10-11 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Inaba, Nagarajan and further in view of Kobayashi.

As demonstrated above, Inaba and Nagarajan, either individually or in combination, do not disclose or suggest the arrangement of the second inductance element as recited in claims 1, 14, 15 and 17, and the second bias circuit as recited in claim 16.

Similarly, Takeshi, Ito and Kobayashi also each fail to disclose or suggest the arrangement of the second inductance element as recited in claims 1, 14, 15 and 17, and the second bias circuit as recited in claim 16.

Consequently, Takeshi, Ito and Kobayashi cannot cure the deficiencies of Inaba and Nagarajan for failing to disclose or suggest all the recited features of claims 1 and 14-17.

Accordingly, no obvious combination of Inaba, Nagarajan, Takeshi, Ito and Kobayashi can result in the subject matter of claims 1 and 14-17, since these references, either individually or in combination, fail to disclose or suggest all the recited features of claims 1 and 14-17.

Therefore, Applicants respectfully submit that claims 1 and 14-17, as well as claims 2-13 and 18-22 which depend therefrom, are patentable over the applied references.

Dependent claims 2-13 and 18-22 recite further distinguishing features over the applied references, and are also patentable by virtue of depending form claims 1 and 14-17. The foregoing explanation of the patentability of independent claims 1 and 14-17 is sufficiently clear such that it is believed to be unnecessary to separately demonstrate the additional patentable features of the dependent claims at this time. However, Applicants reserve the right to do should it become appropriate.

II. Conclusion

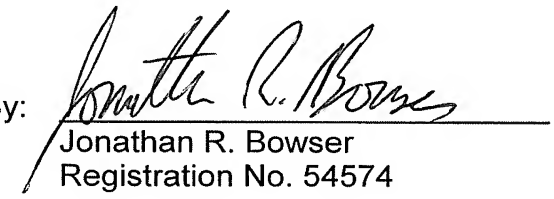
In view of the foregoing amendments and remarks, it is respectfully submitted that the present application is clearly in condition for allowance. Accordingly, favorable examination and consideration of the instant application are respectfully requested.

If, after reviewing this Amendment, the Examiner feels there are any issues remaining which must be resolved before the application can be passed to issue, the Examiner is respectfully requested to contact the undersigned by telephone in order to resolve such issues.

Respectfully submitted,

BUCHANAN INGERSOLL & ROONEY PC

Date: April 27, 2009

By: 
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